REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-14 are presently active in this case, Claims 1 and 2 having been amended and Claims 6-14 having been added by way of the present Amendment.

The amendments and additions to the claims are fully supported by the disclosure of the present application, for example, on page 5, line 9, through page 6, line 24, page 7, lines 15-18, page 7, lines 24-26, and the corresponding figures.

In the outstanding Official Action, Claims 1-5 were rejected under 35 U.S.C. 102(b) as being anticipated by, or in the alternative, under 35 U.S.C. 103(a) as obvious of Gerber et al. (U.S. Patent No. 5,401,913). Claims 1-5 were rejected under 35 U.S.C. 103(a) as being unpatentable over Gerber et al. in view of either one of Furukawa et al. (JP 08293677), Bohn (U.S. Patent No. 6,537,412), or Johnston (U.S. Patent No. 5,153,050). For the reasons discussed below, the Applicant requests the withdrawal of the art rejections.

The basic requirements for establishing a *prima facie* case of obviousness as set forth in MPEP 2143 include (1) there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings, (2) there must be a reasonable expectation of success, and (3) the reference (or references when combined) must teach or suggest all of the claim limitations. The Applicant submits that a *prima facie* case of obviousness has not been established in the present case because the references, either taken singularly or in combination, do not teach or suggest all of the claim limitations.

Claim 1 of the present application recites a method of manufacturing a multilayer circuit board, in which a plurality of printed boards are stacked and pressed into a multilayer circuit board, where each printed board has a conductor layer on one side of an insulating layer. The method comprises preparing a plurality of printed boards with respective copper foils, each printed board being made through the step of forming a via hole in an insulating substrate by laser processing from an insulating layer side so that the via hole extends in a direction of thickness of the insulating substrate so as to reach the conductive layer. The insulating substrate comprises a one-side copper-clad laminate wherein a plated conductor is formed in the via hole, a conductive bump is formed on the plated conductor, and a bonding layer is formed at the insulating layer side. The method also includes etching the copper foil of at least one printed board of the plurality of printed boards so that a printed board with a conductor circuit is formed, and stacking the printed board with the conductor circuit and a second printed board of the plurality of printed boards, wherein the insulating layer side of the second printed board faces the etched copper foil of the printed board with the conductor circuit. The method further includes stacking an outermost conductor layer made of a copper foil on the insulating layer side of the printed board with the conductor circuit with a bonding layer being interposed therebetween, and integrating the outermost conductor layer, the printed board with the conductor circuit, and the second printed board by one time of pressing and thereafter, etching the copper foils on opposite surfaces, thereby obtaining the multilayer circuit board.

The present invention provides an advantageous structure in which it is possible to obtain a multilayer circuit board having any layer inner via holes with high density and high

connecting reliability. Consequently, an electrical signal can be taken out from inner layers through the inner via holes to the conductor circuits at the opposite surfaces.

The Gerber et al. reference describes a method comprising forming a via hole in a circuit board (10). The via hole is filled with a via metal (2), and the via metal is plated with a low melting point metal (22). The circuit board layers include trace metal layers (16) that provide the electrical traces which will interconnect components when they are placed in the completed multi-layer circuit board. Following completion of the formation of the circuit board layers, the layers of circuit boards are stacked and laminated together under heat and pressure. (Column 6, lines 4-6 and 12-15.)

As noted in the Official Action, the Gerber et al. reference does not depict an upper outermost copper conductor layer, as is evident from a review of the drawings. Furthermore, the Applicant submits that the Gerber et al. reference does not disclose a step of etching the copper foils on opposite surfaces after integrating layers of the multilayer circuit board, as recited in Claim 1 of the present application. As noted in column 6, lines 4-6, of the Gerber et al. reference, the stacking and lamination only occurs after the circuit board layers are completed. Such completion includes formation of the trace metal layers (34, 36, 38, 40) and various cover metal layers (50, 52, 54, 56). Accordingly, the Gerber et al. reference does not disclose stacking an outermost conductor layer made of a copper foil on the insulating layer side of the printed board with the conductor circuit with a bonding layer being interposed therebetween, and integrating the outermost conductor layer, the printed board with the conductor circuit, and the second printed board by one time of pressing *and thereafter, etching the copper foils on opposite surfaces*, as expressly recited in amended Claim 1.

Conductive circuits can be formed on both sides of the outermost layer in the claimed invention (see FIG. 3 of the present application), whereas the insulating base material (designated by 74 in FIG. 11 of the Gerber et al. reference) prevents formation of a circuit on one side of the outermost conductive layer (78). As a result, a signal can be supplied into and derived from both sides in the claimed invention but in the Gerber et al. reference, a signal can be supplied into and derived from one side of the conductive layer.

Accordingly, the Applicant respectfully submits that the Gerber et al. reference does not anticipate or render obvious Claim 1 of the present application. Therefore, the Applicant respectfully requests the withdrawal of the anticipation and obviousness rejection of Claim 1 in view of the Gerber et al. reference.

Furthermore, the Applicant respectfully submits that the Fukukawa et al. reference, the Bohn reference, and the Johnston reference fail to supplement the deficiencies in the teachings of the Gerber et al. reference discussed above.

The Fukukawa et al. reference describes an inner-layer circuit board (3) having faces on which a resin insulating layer (2) and conductive bumps (4) are formed. A copper foiled adhesive layer (1) coated with an adhesive layer (1a) are stacked, and the stacked body is heated and pressed to form an integral body. A group of conductive bumps break through the copper foiled adhesive layer (1a) and then are connected to a face of the copper foil (1). Non-connected sections of the inner-layer circuit (5) are covered with the resin insulating layer (2).

The Fukukawa et al. reference does not disclose stacking an outermost conductor layer made of a copper foil on the insulating layer side of a printed board with the conductor

circuit with a bonding layer being interposed therebetween, and integrating the outermost conductor layer, the printed board with the conductor circuit, and a second printed board by one time of pressing *and thereafter, etching the copper foils on opposite surfaces*, as expressly recited in amended Claim 1. The Fukukawa et al. reference does not disclose etching the copper foil (1) after integrating the printed wiring board. Accordingly, the Fukukawa et al. reference does not supplement the deficiencies in the Gerber et al. reference discussed above.

The Bohn reference describes a multilayer (1) including an upper outer layer (2a) and a lower outer layer (2b), which are made of metal foils, two inner layers (3), which are equipped with strip conductors (3a), and three intermediate layers (4) impregnated with adhesive, which are arranged respectively between the layers mentioned.

The Bohn reference does not disclose stacking an outermost conductor layer made of a copper foil on the insulating layer side of a printed board with the conductor circuit with a bonding layer being interposed therebetween, and integrating the outermost conductor layer, the printed board with the conductor circuit, and a second printed board by one time of pressing *and thereafter, etching the copper foils on opposite surfaces*, as expressly recited in amended Claim 1. The Bohn reference does not disclose etching the metal foils on opposite surfaces after integrating the multilayer. Accordingly, the Bohn reference does not supplement the deficiencies in the Gerber et al. reference discussed above.

The Johnston reference describes a copper foil layer (4) placed on a separator sheet (2). Upon the copper is placed a laminated multilayer core (10) including three double plies (12) of prepreg and two double sided boards (14) pre-etched with conductive paths (15) on

both surfaces. Upon this inner core laminated (10) is another sheet of copper foil (4). The upper and lower copper foils (4) are described as the working surfaces of the first PC board in the stack. They are also described as being etched to produce conductive paths when the board is finished. Then another board is layered upon the first (see column 4, lines 49-57) in order to make a six layer multilayer board.

The Johnston reference does not disclose stacking an outermost conductor layer made of a copper foil on the insulating layer side of a printed board with the conductor circuit with a bonding layer being interposed therebetween, and integrating the outermost conductor layer, the printed board with the conductor circuit, and a second printed board by one time of pressing *and thereafter, etching the copper foils on opposite surfaces*, as expressly recited in amended Claim 1. The Johnston reference does not disclose etching the metal foils on opposite surfaces after integrating the multilayer board, but rather each individual board is etched and then the board is assembled. Accordingly, the Johnston reference does not supplement the deficiencies in the Gerber et al. reference discussed above.

Accordingly, the Applicant respectfully requests the withdrawal of the obviousness rejection of Claim 1.

Claims 2-9 are considered allowable for the reasons advanced for Claim 1 from which they depend. These claims are further considered allowable as they recite other features of the invention that are neither disclosed, taught, nor suggested by the applied references when those features are considered within the context of Claim 1.

Newly added Claims 10-14 are considered allowable as they recite features of the invention that are neither disclosed nor suggested by the references of record. For example,

new Claim 10 recites a method of manufacturing a multilayer circuit board, in which a plurality of printed boards are stacked and pressed into a multilayer circuit board, where each printed board has a via hole extending through the insulate ng substrate to the conductor layer, the via hole is filled with a plated conductor, and the plated conductor filling the via hole has an amount determined so that the plated conductor does not extend above the surface of the insulating substrate. Such features are not disclosed in the Gerber et al. reference, which, for example, includes via metal (20) that extends above the surface of circuit board (10). The other cited references do not supplement the deficiencies in the teaching of the Gerber et al. reference. Claims 11-14 are allowable for at least the reasons presented for Claim 10, from which they depend.

Consequently, in view of the above discussion, it is respectfully submitted that the present application is in condition for formal allowance and an early and favorable reconsideration of this application is therefore requested.

Respectfully Submitted,

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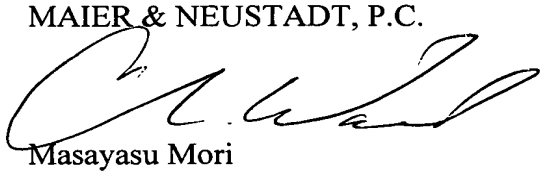

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